REMARKS/ARGUMENTS

Applicant is pleased to know that the Examiner has indicated that claims 16-18 and 27 are directed towards patentable subject matter. (It is noted that claims 28 and 29 depend from claim 27 and are therefore also directed towards patentable subject matter.) Applicant has re-written claims 16-18 and 27-29 as new claims 35-40, respectively.

Applicant has also submitted a new claim 34 which requires the simultaneous formation of a pad layer and a wiring layer in the various layers of the semiconductor device. The remaining claims have been amended to include this limitation. It is believed that these limitations, in combination with the remaining limitations of the claims, are neither disclosed nor suggested in the art of record.

With respect to claims 22 and 33, the Examiner has rejected these claims as indefinite on the grounds that the claims do not specify where the layers are formed. However, this does not make the claims indefinite. Rather, it makes them broad. The claims cover a process for forming the conductive pad which includes each of the sub-steps set forth in the claims, irrespective of the specific location of the layers being formed (as long as the layers together form the claimed conductive pad). Accordingly, it is requested the Examiner's rejection on this ground be withdrawn.

Reconsideration and allowance of the application are earnestly solicited.

Dated: March 18, 2003

Respectfully submitted,

By _____

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APPENDIX A
Version With Markings To Show Changes Made
37 C.F.R. § 1.121(b)(1)(iii) AND (c)(1)(ii)

CLAIMS:

20. (Amended) A method of manufacturing a semiconductor device according to claim 23, wherein the step (e) comprises:

forming Ti films covering inner surfaces of the through holes in the first interlayer insulating film by sputtering;

forming TiN layers on the Ti films by sputtering; and

forming W layers on the TiN layers.

23. (Amended) A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) simultaneously forming a first conductive pad and a first wiring layer on the insulating film;

(c) forming a first interlayer insulating film on [both] the first conductive pad, the first wiring layer and the insulating film;

(d) forming a plurality of first through holes in the first interlayer insulating film, each of the first through holes extending from the first conductive pad or the first wiring layer respectively, to an upper surface of the first interlayer insulating film;

(e) filling the plurality of first though holes with conductive material;

(f) simultaneously forming a second conductive pad and a second wiring layer on the first interlayer insulating film, each of the second conductive pad and the second wiring layer being in contact with the conductive material in one or more of the plurality of first through holes;

(g) forming a second interlayer insulating film on [both] the second conductive pad, the second wiring layer and the first interlayer insulating film;

(h) forming a plurality of second through holes in the second interlayer insulating film, each of the first through holes extending from the second conductive pad or the second wiring layer, respectively, to an upper surface of the second interlayer insulating film;

(i) filling the plurality of second through holes formed in the second interlayer insulating film with conductive material;

(j) simultaneously forming a third conductive pad and a third wring layer on the second interlayer insulating film, each of the third conductive pad and wiring layer being [and] in contact with the conductive material in one or more of the second through holes formed in the second interlayer insulating film;

(k) forming a third interlayer insulating film on both the third conductive pad and the second interlayer insulating film;

(l) forming a through hole through the third interlayer insulating film which is substantially the same size as the third conductive pad; and

(m) forming a bonding pad on the third conductive pad in the through hole in the third interlayer insulating film.

24. (Amended) A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a base layer over the insulating film by carrying out at least the following acts:

(1) simultaneously forming a conductive pad and a wiring layer on the insulating film;

(2) forming a base layer insulating film on [both] the conductive pad, the wiring layer and the insulating film;

(3) forming a plurality of base through holes in the base layer insulating film, each of the [which] through base holes extending [extend] from the conductive pad or the wiring layer, respectively, to an upper surface of the base layer insulating film;

(4) filling the base through [though] holes with a conductive material;

(c) forming first through nth intermediate layers over the base layer, n being a positive integer greater than 1, the first intermediate layer being formed on the base layer, the remaining intermediate layers being formed one on top of the other, each of the respective intermediate layers being formed by carrying out at least the following steps:

(1) simultaneously forming a conductive pad and a wiring layer on the insulating film of the immediately preceding layer, each of the

conductive pad and wiring layer being in contact with the conductive material in one or more of the through holes of the immediately preceding layer;

(2) forming a respective interlayer insulating film on [both] the conductive pad, the wiring layer and the insulating film of the immediately preceding layer;

(3) forming a plurality of through holes in the interlayer insulating film of the respective intermediate layer, each of the through holes extending from the conductive pad or wiring layer, respectively, of the respective intermediate layer to an upper surface of the interlayer insulating film of the respective intermediate layer;

(4) filling each of the through holes of the respective intermediate layer with a conductive material; and

(d) forming an upper layer on the nth intermediate layer by carrying out at least the following steps:

(1) forming a conductive pad on the interlayer insulating film of the nth intermediate layer in contact with the conductive material in that [the] plurality of through holes in the insulating film of the nth intermediate layer which are in contact with the conductive pad of the nth intermediate layer;

(2) forming an upper layer insulating film on both the conductive pad of the upper layer and the insulating film of the nth intermediate layer;

(3) forming an upper through hole through the upper layer insulating film, said upper through hole being substantially the same size as the conductive pad of the upper layer; and

(4) forming a bonding pad on the conductive pad of the upper layer, the bonding pad being located in the upper through hole in the upper layer insulating film.

33. (Amended) A method of manufacturing a semiconductor device according to claim 24, wherein the step (c)(1) of forming the conductive pad comprises:

forming a Ti layer;

forming an Al-Cu alloy layer;

forming a Ti layer; and

forming a TiN layer.

34. (NEW) A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a multi-level sub-structure on an underlying insulating layer which is formed over a semiconductor substrate by repeating the steps of;

(1) forming a conductive layer;

(2) patterning the conductive layer to leave a wiring region and a pad region;

(3) forming an insulating layer over the patterned wiring and pad regions;

(4) forming a wiring via hole through the insulating layer above the wiring region and a plurality of pad via holes through the insulating layer above the pad region;

(5) embedding the via holes with conductive material to form a wiring via connected to said wiring region and a plurality of pad vias connected to said pad region;

(b) forming an upper conductive layer on a surface of the multi-level sub-structure;

(c) patterning the upper conductive layer to leave an upper wiring region and an upper pad region;

(d) forming an upper insulating layer over the upper wiring region and the upper pad region;

(e) forming an upper wiring via hole through the upper insulating layer above the upper wiring region and an opening which exposes a central region of the upper pad region encompassing a region above said plurality of pad vias;

(f) forming an uppermost wiring region connected to said upper wiring region and an uppermost pad region connected to said upper pad region,

wherein the wiring regions and the pad regions are respectively vertically registered.

35. (NEW) A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a first conductive pad on the insulating film;

(c) forming a first interlayer insulating film on both the first conductive pad and the insulating film;

(d) forming a plurality of first through holes in the first interlayer insulating film extending from the first conductive pad to an upper surface of the first interlayer insulating film;

(e) filling the plurality of first though holes with conductive material;

(f) forming a second conductive pad on the first interlayer insulating film [and] in contact with the conductive material in the plurality of first through holes;

(g) forming a second interlayer insulating film on both the second conductive pad and the first interlayer insulating film;

(h) forming a plurality of second through holes in the second interlayer insulating film extending from the second conductive pad to an upper surface of the second interlayer insulating film;

(i) filling the plurality of second through holes formed in the second interlayer insulating film with conductive material;

(j) forming a third conductive pad on the second interlayer insulating film and in contact with the conductive material in the second through holes formed in the second interlayer insulating film;

(k) forming a third interlayer insulating film on both the third conductive pad and the second interlayer insulating film;

(l) forming a through hole through the third interlayer insulating film which is substantially the same size as the third conductive pad; and

(m) forming a bonding pad on the third conductive pad in the through hole in the third interlayer insulating film.

wherein the step (c) of forming the first interlayer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin on the first silicon oxide film;

thermally treating the hydrogen silsesquioxane resin to form a ceramic silicon oxide film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

36. (NEW) A method of manufacturing a semiconductor device according to claim 35, further comprising a step of planarizing the second silicon oxide film by CMP.

37. (NEW) A method of manufacturing a semiconductor device according to claim 35, further comprising a step of planarizing the second silicon oxide film by etching.

38. (NEW) A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a base layer over the insulating film by carrying out at least the following acts:

(1) forming a conductive pad on the insulating film;

(2) forming a base layer insulating film on both the conductive pad and the insulating film;

(3) forming a plurality of base through holes in the base layer insulating film which through holes extend from the conductive pad to an upper surface of the base layer insulating film;

(4) filling the base though holes with a conductive material;

(c) forming first through nth intermediate layers over the base layer, n being a positive integer greater than 1, the first intermediate layer being formed on the base layer, the remaining intermediate layers being formed one on top of the other, each of the respective intermediate layers being formed by carrying out at least the following steps:

(1) forming a conductive pad on the insulating film of the immediately preceding layer in contact with the conductive material in the through holes of the immediately preceding layer;

(2) forming a respective interlayer insulating film on both the conductive pad and the insulating film of the immediately preceding layer;

(3) forming a plurality of through holes in the interlayer insulating film of the respective intermediate layer, the through holes extending from the conductive pad of the respective intermediate

layer to an upper surface of the interlayer insulating film of the respective intermediate layer;

(4) filling each of the through holes of the respective intermediate layer with a conductive material; and

(d) forming an upper layer on the nth intermediate layer by carrying out at least the following steps:

(1) forming a conductive pad on the interlayer insulating film of the nth intermediate layer in contact with the conductive material in the plurality of through holes in the insulating film of the nth intermediate layer;

(2) forming an upper layer insulating film on both the conductive pad of the upper layer and the insulating film of the nth intermediate layer;

(3) forming an upper through hole through the upper layer insulating film, said upper through hole being substantially the same size as the conductive pad of the upper layer; and

(4) forming a bonding pad on the conductive pad of the upper layer, the bonding pad being located in the upper through hole in the upper layer insulating film.

wherein the step (b)(2) of forming the base layer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin on the silicon oxide film;

thermally treating the hydrogen silsesquioxane to form a ceramic silicon oxide film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

39. (NEW) A method of manufacturing a semiconductor device according to claim 38, further comprising a step of planarizing the second silicon oxide film by CMP.

40. (NEW) A method of manufacturing a semiconductor device according to claim 38, further comprising a step of planarizing the second silicon oxide film by etching.

APPENDIX B

CLEAN VERSION WITHOUT AMENDED/NEW INDICATIONS
37 C.F.R. § 1.121 (c)(3)

CLAIMS:

20. A method of manufacturing a semiconductor device according to claim 23, wherein the step (e) comprises:

forming Ti films covering inner surfaces of the through holes in the first interlayer insulating film by sputtering;

forming TiN layers on the Ti films by sputtering; and

forming W layers on the TiN layers.

23. A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) simultaneously forming a first conductive pad and a first wiring layer on the insulating film;

(c) forming a first interlayer insulating film on [both] the first conductive pad, the first wiring layer and the insulating film;

(d) forming a plurality of first through holes in the first interlayer insulating film, each of the first through holes extending from the first conductive pad or the first wiring layer respectively, to an upper surface of the first interlayer insulating film;

(e) filling the plurality of first though holes with conductive material;

(f) simultaneously forming a second conductive pad and a second wiring layer on the first interlayer insulating film, each of the second conductive pad and the second wiring layer being in contact with the conductive material in one or more of the plurality of first through holes;

(g) forming a second interlayer insulating film on the second conductive pad, the second wiring layer and the first interlayer insulating film;

(h) forming a plurality of second through holes in the second interlayer insulating film, each of the first through holes extending from the second conductive pad or the second wiring layer, respectively, to an upper surface of the second interlayer insulating film;

(i) filling the plurality of second through holes formed in the second interlayer insulating film with conductive material;

(j) simultaneously forming a third conductive pad and a third wring layer on the second interlayer insulating film, each of the third conductive pad and wiring layer being in contact with the conductive material in one or more of the second through holes formed in the second interlayer insulating film;

(k) forming a third interlayer insulating film on both the third conductive pad and the second interlayer insulating film;

(l) forming a through hole through the third interlayer insulating film which is substantially the same size as the third conductive pad; and

(m) forming a bonding pad on the third conductive pad in the through hole in the third interlayer insulating film.

24. A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a base layer over the insulating film by carrying out at least the following acts:

(1) simultaneously forming a conductive pad and a wiring layer on the insulating film;

(2) forming a base layer insulating film on the conductive pad, the wiring layer and the insulating film;

(3 forming a plurality of base through holes in the base layer insulating film, each of the through base holes extending from the conductive pad or the wiring layer, respectively, to an upper surface of the base layer insulating film;

(4) filling the base through holes with a conductive material;

(c) forming first through nth intermediate layers over the base layer, n being a positive integer greater than 1, the first intermediate layer being formed on the base layer, the remaining intermediate layers being formed one on top of the other, each of the respective intermediate layers being formed by carrying out at least the following steps:

(1) simultaneously forming a conductive pad and a wiring layer on the insulating film of the immediately preceding layer, each of the

conductive pad and wiring layer being in contact with the conductive material in one or more of the through holes of the immediately preceding layer;

(2) forming a respective interlayer insulating film on the conductive pad, the wiring layer and the insulating film of the immediately preceding layer;

(3) forming a plurality of through holes in the interlayer insulating film of the respective intermediate layer, each of the through holes extending from the conductive pad or wiring layer, respectively, of the respective intermediate layer to an upper surface of the interlayer insulating film of the respective intermediate layer;

(4) filling each of the through holes of the respective intermediate layer with a conductive material; and

(d) forming an upper layer on the nth intermediate layer by carrying out at least the following steps:

D2 cont'd

(1) forming a conductive pad on the interlayer insulating film of the nth intermediate layer in contact with the conductive material in that plurality of through holes in the insulating film of the nth intermediate layer which are in contact with the conductive pad of the nth intermediate layer;

(2) forming an upper layer insulating film on both the conductive pad of the upper layer and the insulating film of the nth intermediate layer;

(3) forming an upper through hole through the upper layer insulating film, said upper through hole being substantially the same size as the conductive pad of the upper layer; and

(4) forming a bonding pad on the conductive pad of the upper layer, the bonding pad being located in the upper through hole in the upper layer insulating film.

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33. A method of manufacturing a semiconductor device according to claim 24,

D3 cont

wherein the step (c)(1) of forming the conductive pad comprises:

forming a Ti layer;

forming an Al-Cu alloy layer;

D3 cancel

forming a Ti layer; and

forming a TiN layer.

34. (NEW) A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a multi-level sub-structure on an underlying insulating layer which is formed over a semiconductor substrate by repeating the steps of;

(1) forming a conductive layer;

(2) patterning the conductive layer to leave a wiring region and a pad region;

D4

(3) forming an insulating layer over the patterned wiring and pad regions;

(4) forming a wiring via hole through the insulating layer above the wiring region and a plurality of pad via holes through the insulating layer above the pad region;

(5) embedding the via holes with conductive material to form a wiring via connected to said wiring region and a plurality of pad vias connected to said pad region;

(b) forming an upper conductive layer on a surface of the multi-level sub-structure;

(c) patterning the upper conductive layer to leave an upper wiring region and an upper pad region;

(d) forming an upper insulating layer over the upper wiring region and the upper pad region;

(e) forming an upper wiring via hole through the upper insulating layer above the upper wiring region and an opening which exposes a central region of the upper pad region encompassing a region above said plurality of pad vias;

(f) forming an uppermost wiring region connected to said upper wiring region and an uppermost pad region connected to said upper pad region,

wherein the wiring regions and the pad regions are respectively vertically registered.

35. A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a first conductive pad on the insulating film;

(c) forming a first interlayer insulating film on both the first conductive pad and the insulating film;

(d) forming a plurality of first through holes in the first interlayer insulating film extending from the first conductive pad to an upper surface of the first interlayer insulating film;

(e) filling the plurality of first though holes with conductive material;

(f) forming a second conductive pad on the first interlayer insulating film [and] in contact with the conductive material in the plurality of first through holes;

(g) forming a second interlayer insulating film on both the second conductive pad and the first interlayer insulating film;

(h) forming a plurality of second through holes in the second interlayer insulating film extending from the second conductive pad to an upper surface of the second interlayer insulating film;

(i) filling the plurality of second through holes formed in the second interlayer insulating film with conductive material;

(j) forming a third conductive pad on the second interlayer insulating film and in contact with the conductive material in the second through holes formed in the second interlayer insulating film;

(k) forming a third interlayer insulating film on both the third conductive pad and the second interlayer insulating film;

(l) forming a through hole through the third interlayer insulating film which is substantially the same size as the third conductive pad; and

(m) forming a bonding pad on the third conductive pad in the through hole in the third interlayer insulating film.

wherein the step (c) of forming the first interlayer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin on the first silicon oxide film;

thermally treating the hydrogen silsesquioxane resin to form a ceramic silicon oxide film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

36. (NEW) A method of manufacturing a semiconductor device according to claim 35, further comprising a step of planarizing the second silicon oxide film by CMP.

37. (NEW) A method of manufacturing a semiconductor device according to claim 35, further comprising a step of planarizing the second silicon oxide film by etching.

38. A method of manufacturing a semiconductor device, the method comprising the steps of:

(a) forming an insulating film on a semiconductor substrate;

(b) forming a base layer over the insulating film by carrying out at least the following acts:

(1) forming a conductive pad on the insulating film;

(2) forming a base layer insulating film on both the conductive pad and the insulating film;

(3) forming a plurality of base through holes in the base layer insulating film which through holes extend from the conductive pad to an upper surface of the base layer insulating film;

(4) filling the base though holes with a conductive material;

(c) forming first through nth intermediate layers over the base layer, n being a positive integer greater than 1, the first intermediate layer being formed on the base layer, the remaining intermediate layers being formed one on top of the other, each of the respective intermediate layers being formed by carrying out at least the following steps:

(1) forming a conductive pad on the insulating film of the immediately preceding layer in contact with the conductive material in the through holes of the immediately preceding layer;

(2) forming a respective interlayer insulating film on both the conductive pad and the insulating film of the immediately preceding layer;

(3) forming a plurality of through holes in the interlayer insulating film of the respective intermediate layer, the through holes extending from the conductive pad of the respective intermediate

layer to an upper surface of the interlayer insulating film of the respective intermediate layer;

(4) filling each of the through holes of the respective intermediate layer with a conductive material; and

(d) forming an upper layer on the nth intermediate layer by carrying out at least the following steps:

(1) forming a conductive pad on the interlayer insulating film of the nth intermediate layer in contact with the conductive material in the plurality of through holes in the insulating film of the nth intermediate layer;

(2) forming an upper layer insulating film on both the conductive pad of the upper layer and the insulating film of the nth intermediate layer;

(3) forming an upper through hole through the upper layer insulating film, said upper through hole being substantially the same size as the conductive pad of the upper layer; and

(4) forming a bonding pad on the conductive pad of the upper layer, the bonding pad being located in the upper through hole in the upper layer insulating film.

wherein the step (b)(2) of forming the base layer insulating film comprises:

forming a first silicon oxide film;

coating hydrogen silsesquioxane resin on the silicon oxide film;

thermally treating the hydrogen silsesquioxane to form a ceramic silicon oxide film; and

forming a second silicon oxide film on the ceramic silicon oxide film by plasma CVD.

39. A method of manufacturing a semiconductor device according to claim 38, further comprising a step of planarizing the second silicon oxide film by CMP.

40. (NEW) A method of manufacturing a semiconductor device according to claim 38, further comprising a step of planarizing the second silicon oxide film by etching.